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02/21/02

PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10078340	FILING DATE 02/21/2002	CLASS 997	SUBCLASS	GAU 233 2211	EXAMINER
<b>**APPLICANTS:</b> Tomita Hiroyoshi;					
<b>**CONTINUING DATA VERIFIED:</b> THIS APPLICATION IS A DIV OF 09/587,296 06/05/2000 PAT 6,373,783					
<b>** FOREIGN APPLICATIONS VERIFIED:</b> JAPAN HEI 11-310036 10/29/1999					
PG-PUB <input type="checkbox"/>		DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>	
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no Verified and Acknowledged Examiners's initials				ATTORNEY DOCKET NO 108397-00067	
TITLE : Semiconductor integrated circuit, method of controlling the same, and variable delay circuit					

U.S. DEPT. OF COMM./PAT. & TM-PTO-435L (Rev. 12-94)

<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Total Claims	
		Print Claim for O.G.	
<b>ISSUE FEE</b>		<b>DRAWING</b>	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
		Print Fig.	
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		<b>Application Examiner</b>	
		<b>PREPARED FOR ISSUE</b>	
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